Technická univerzita v Košiciach
Fakulta elektrotechniky a informatiky
Laboratórium priemyselného inžinierstva

DIPLOMOVÁ PRÁCA

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Prekladač z VHDL-AMS-RT do Matlabu pre simuláciu v reálnom čase

Vedúci diplomovej práce:
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DIPLOMA THESIS

Author: **Peter KEHL**
Specialization: Industrial Engineering
Title: **Translator from VHDL-AMS-RT to Matlab for Real-Time simulation**

Task:

Analyze development process of application for RT simulation by means of VHDL-AMS-RT language integrated with Simulink. Choose most used subset of VHDL-AMS-RT with focus on analog and mixed signals. Create:

- translator from VHDL-AMS to C++ that leaves semantical checking to C++ compilator
- libraries and integration tool for connection with Simulink
- documentation

Supervisor of the thesis: doc. Ing. Michal Girman, PhD. - TU Košice
Ing. Walter Commerell, PhD. - University of Applied Sciences, Ulm, Germany

Date of the assignment of the thesis: 25^{th} March 2002
Date of the submission of the thesis: 6^{th} May 2002

doc. Ing. Michal GIRMAN, PhD.
director of LIE

doc. Ing. Dušan KOCUR, CSc.
dean

Košice 22^{th} March 2002

Prehlásenie o samostatnom vypracovaní DP

Týmto prehlasujem, že som túto diplomovú prácu, vrátane príloh, vypracoval samostatne a uvádzam všetku použitú literatúru.

Declaration about an individual elaboration of the diploma thesis

Hereby I declare that I have elaborated this diploma thesis, including the annexes, individually, and that I have mentioned all the sources used.

Košice 6^{th} May 2002
Peter Kehl

Názov práce: Prekladač z VHDL-AMS-RT do Matlabu pre simuláciu v reálnom čase

Katedra: Laboratórium priemyselného inžinierstva, Fakulta elektrotechniky a informatiky, Technická univerzita v Košiciach

Autor: Peter Kehl

Vedúci DP: Michal Girman, Walter Commerell

Dátum: 6. máj 2002

Kľúčové slová: VHDL-AMS, VHDL-AMS-RT, Simulácia v reálnom čase, C++, JavaCC, Java

Anotácia:

Modelovanie navrhnutých systémov so spojitými, diskrétnymi a zmiešanými signálmi je dnes nutnosťou. VHDL-AMS (IEEE 1076.1) štandardizuje popis viacdoménovych systémov. Vysoko integrované produkty musia byť simulované v spojení s reálnymi súčasťami. To znamená simuláciu v reálnom čase.

Projekt analyzuje a prezentuje prekladač z VHDL-AMS-RT (podmnožina VHDL-AMS pre reálny čas) do C++ využívaný so Simulinkom. Sémantická kontrola je prenechaná na C++ kompilátor v najväčšej možnej miere. Dôraz je na kontinuálne a zmiešané signály, vektory a základné štrukturálne príkazy. Je to ľahko použiteľný nástroj s výkonným simulačným prostredím Simulinku.

Title: Translator from VHDL-AMS-RT to Matlab for Real Time simulation

Department: Laboratory of Industrial Engineering, Faculty of Electrotechnics and Informatics, Technical University, Košice

Author: Peter Kehl

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Date: 6^{th} May 2002

Keywords: VHDL-AMS, VHDL-AMS-RT, Real Time Simulation, Simulink, C++, JavaCC, Java

Anotation:

Modeling of designed systems with continuous, discrete and mixed signals represents a necessity today. VHDL-AMS (IEEE 1076.1) standardizes a multi-domain system description. High integrated products need to be simulated when connected to real components. This involves simulation in Real Time.

The project analyzes and presents a translator from VHDL-AMS-RT (VHDL-AMS subset for REAL-TIME) to C++ for use with Simulink. The semantical checking is left on C++ compiler up to the maximum level. The focus is on continuous and mixed signals, vectors and basic structural statements. It is easy-to-use tool integrated with a powerfull simulation environment of Simulink.

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